12X4 Row-Column Sharing Matrix LED Driver for Full-Color Backlight

Features

- 12 current sink x 4 scans row-column sharing matrix LED driver
- 5 parallel IC configuration drives up to 400 RGB LED pixels or 1200 LEDs
- Supports 5V supply voltage for USB application
- 12 constant-current output channels
  Constant output current range:
  5mA-40mA @ V_{DD}=5V
- Excellent output current accuracy:
  - Between channels: ±1.5% (typ.)
  - Between ICs: ±2.5% (typ.)
- Support standard SPI interface
- 10-bit Grayscale control enables 1.07 billion color per LED pixel
- Internal clock for PWM function
- Embedded MOS switches support up to 1/20 time-multiplexing @ 5 parallel IC configuration
- Support internal/external resister to set constant current source
- Individual current gain control:
  8-bit (256 steps) individual groups of color R/G/B LED current control from 0%~100%
- Device stand-by power saving
- Built-in auto-breath lighting effect with adjustable effect duration
- Overcomes ghosting effect of time-multiplex scanning LED display
- LED open and short error detect function
- Staggered delay of output
- Schmitt trigger input
- TSSOP-28L / QFN-28L package selection
- "Pb-free & Green" Package

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Product Description

The MBIA128 is a general purpose Row-Column Sharing Matrix LED Driver with standard SPI programming interface. Each MBIA128 has 12 constant current driving channels, and up to 4 time-multiplexed scans per IC. With Row-Column sharing the driver IC can be setup in parallel configuration to control up to 400 RGB pixels, or 1200 LEDs (5 ICs in parallel, total of 60 channels and 20 scans). MBIA128 is designed for full color backlit application, such as PC gaming devices, consumer and white goods applications.

MBIA128 with internal PWM clock features a 10-bit grayscale control for each LED, which can create color variation of up to 1.07 billion color per LED pixel. With 8-bit (256-step) Individual current gain, each group of R/G/B color LED can be controlled separately, giving flexibility for brightness adjustments. The driver IC has embedded MOS switches and internal resistor to simplify application design, while also supports the option to use external resistor for constant current adjustments.

MBIA128 has auto-breathe lighting control built-in to the driver IC. Designers can adjust the timing characteristics of output current to achieve various breathe lighting effects. MBIA128 also features de-ghost function, which eliminates the ghosting effect of LED matrix architecture. The device supports open / short, and pixel short detect, and has power saving modes which enables low power consumption during device stand-by.

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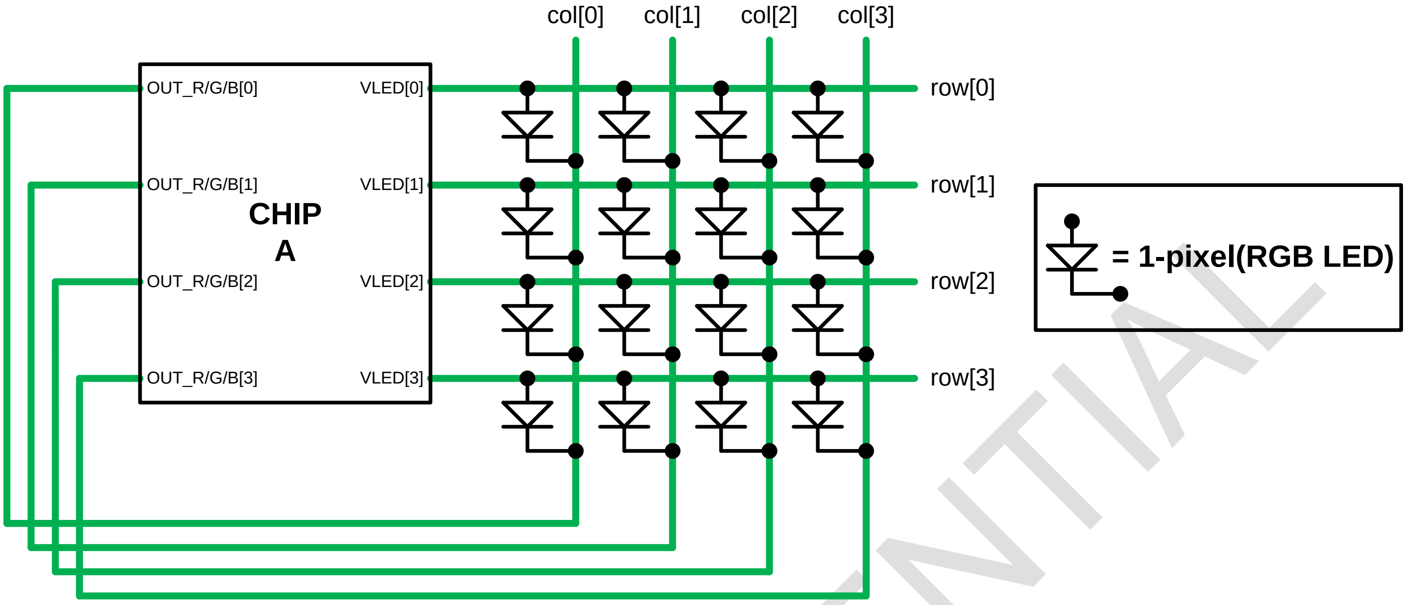
Operation Principle & Application



Typical application circuit (12ch×4s LEDs, 16 RGB pixels)

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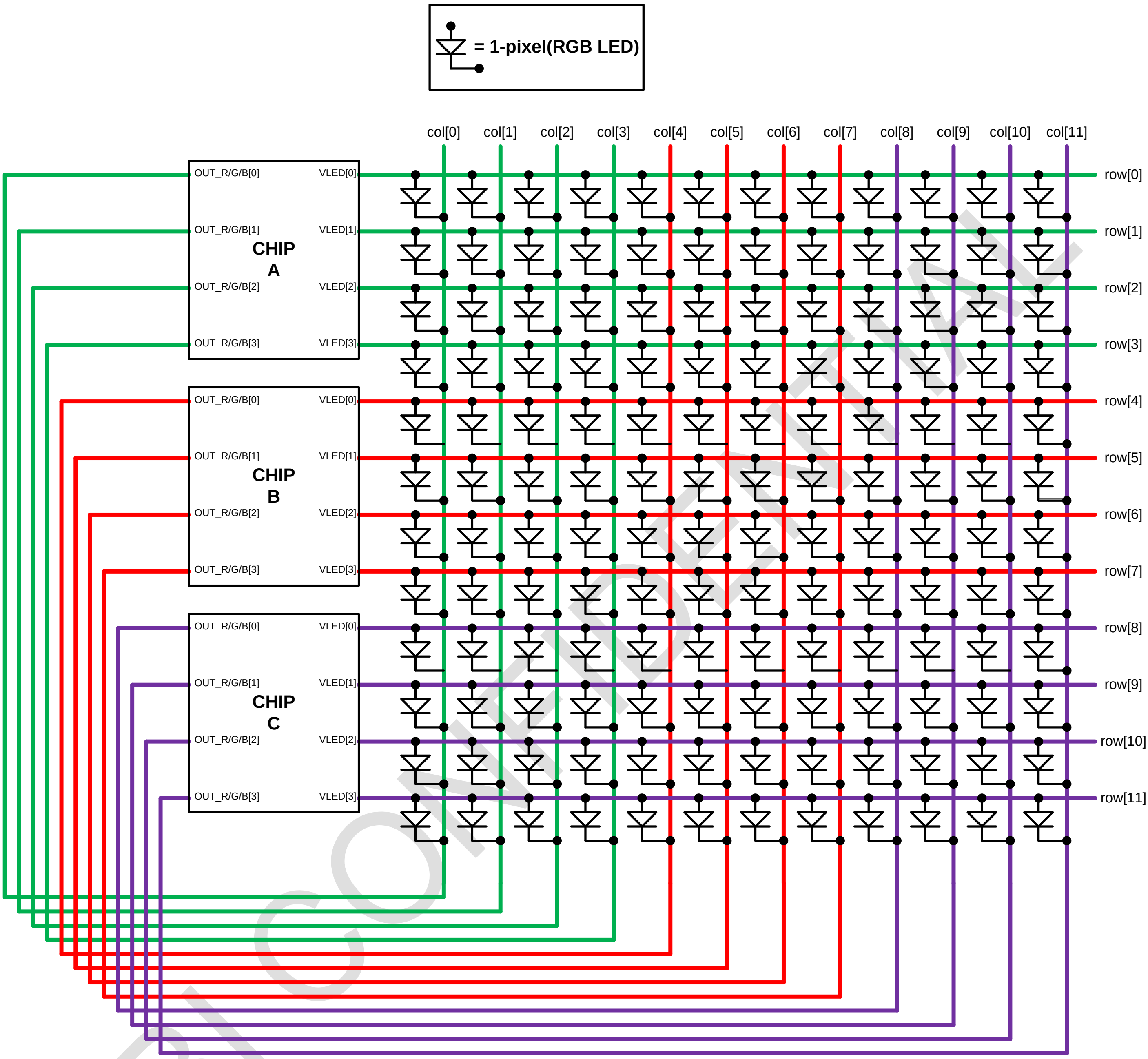
Application for larger RGB LED matrix



(36ch×12s LEDs, 144 RGB pixels)

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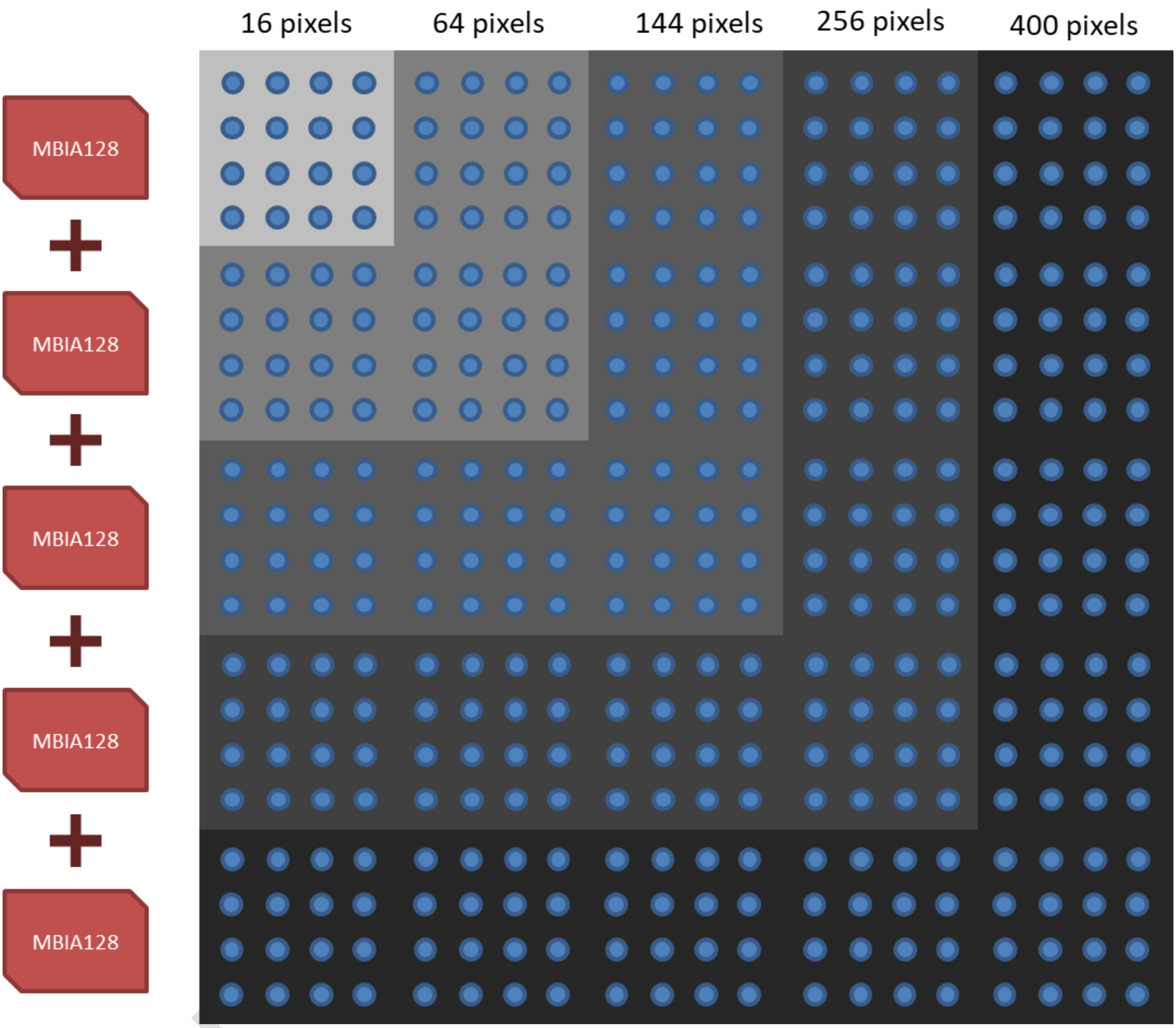
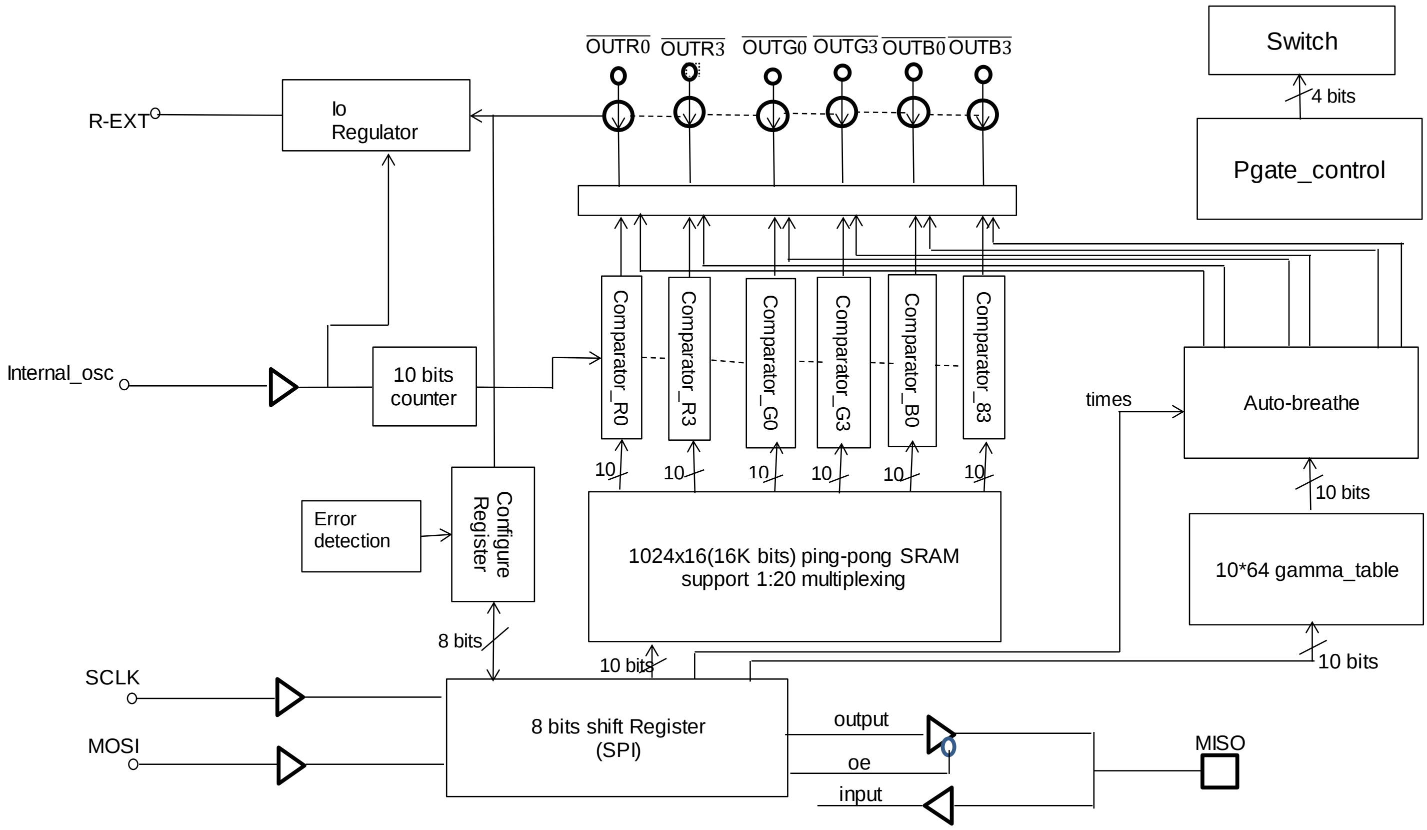
General Application



General application with 1 to 5 MBIA128 (Max 60ch×20s LEDs, 400 RGB pixels)

Block Diagram



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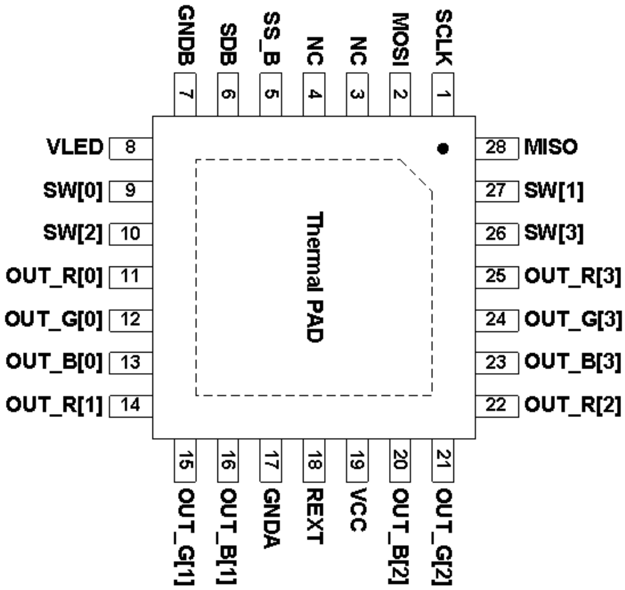
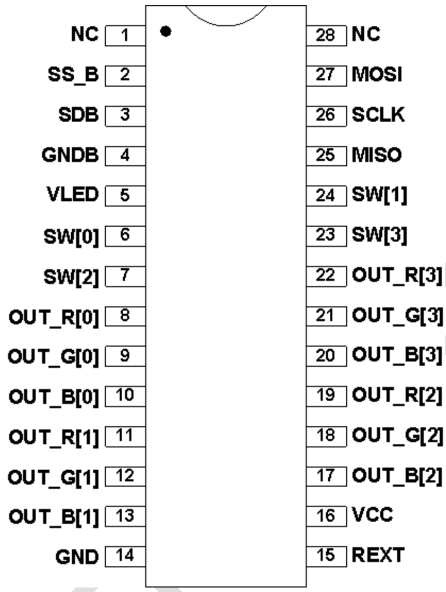
Pin Configuration



(QFN-28-EP)
Top View



(TSSOP-28-EP)
Top View

Terminal Description

Name	Type	Description
VCC	P	Power supply input for internal circuit and matrix driver.
VLED	P	Power supply input for PMOS switch
GNDA	G	Ground pin.(down bound)
GNDB	G	Ground pin.(down bound)
SDB (TCLK)	I	Shutdown the chip when pull to low. (For test clock in test mode)
SCLK	I	SPI data clock input.
SS_B	I	SPI Slave select, low active.
MOSI	I	SPI Master-Output-Slave-Input.
MISO	I/O	SPI Master-Input-Slave-Output. Input/output synchronous signal or clock. In addition to the case of read command is synchronous function.
REXT	I/O	External resistor for constant current setup.
SW[3:0]	O	PMOS switch output for LED matrix scanning.
OUT_R[3:0]	O	Constant current output for "RED" LEDs.
OUT_G[3:0]	O	Constant current output for "GREEN" LEDs.
OUT_B[3:0]	O	Constant current output for "BLUE" LEDs.
Thermal Pad		Need to connect to GND pin
NC[1:0]		No Use

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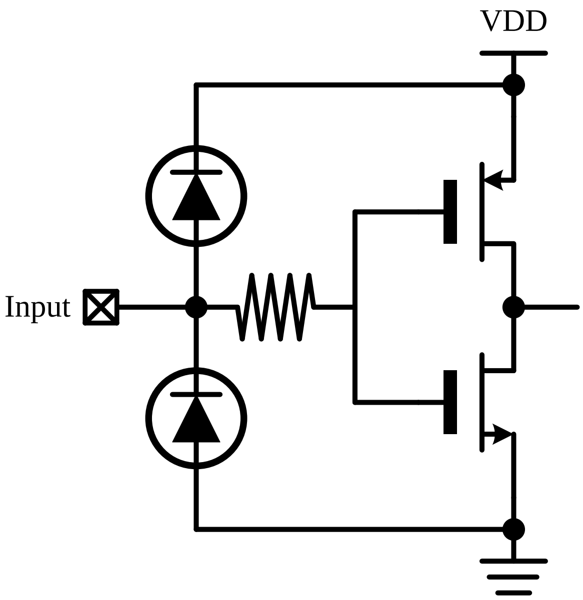
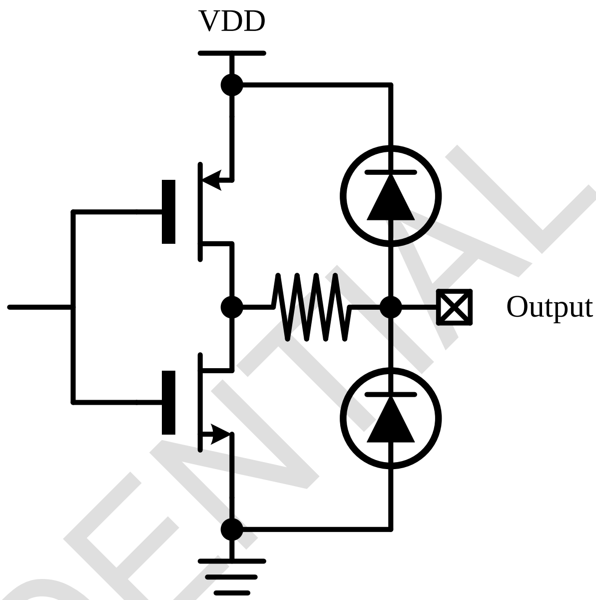
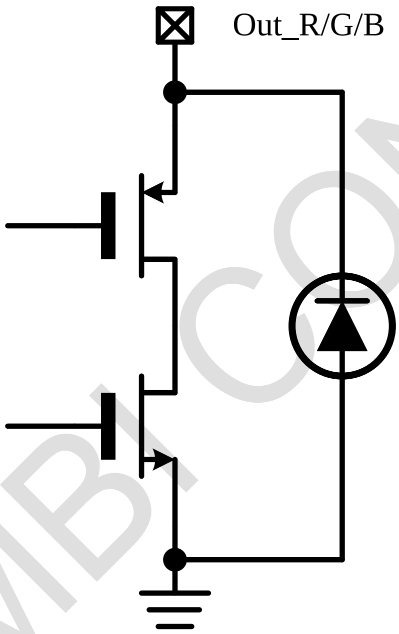
Equivalent Circuits of Inputs and Outputs



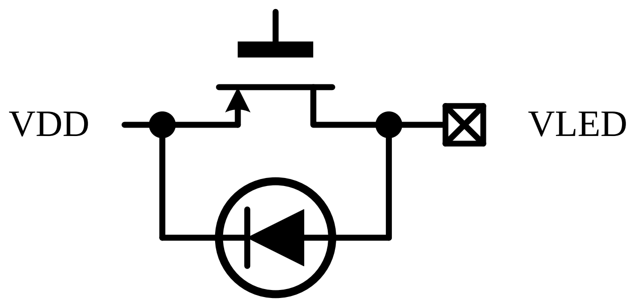
Data Input terminal



Data Output terminal



Current Outputs terminal



Switch Output terminal

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Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	-0.3 ~ +5.5	V
Input Voltage		V_{IN}	-0.2 ~ V_{DD}+0.2	V
Output Current per Output Channel		I_{OUT}	+40	mA
Sustaining Voltage at OUT port		V_{OUT}	-0.3 ~ + V_{DD}+0.3	V
GND Terminal Current		I_{GND}	2000	mA
Power Dissipation	TSSOP-28	$P_D(T_a$=25°C)	TBD	W
		$P_D(T_a$=85°C)	TBD	
	QFN-EP	$P_D(T_a$=25°C)	TBD	
		$P_D(T_a$=85°C)	TBD	
Thermal Resistance, junction to ambient	TSSOP-28	$\theta_{(j-a)}$	TBD	°C/W
	QFN-EP	$\theta_{(j-a)}$	TBD	
Operating Ambient Temperature		T_{opr}	-40~+125	°C
Storage Temperature		T_{stg}	-55~+150	°C

*Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

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Electrical Characteristics (V_{DD}= 5.0V, Ta=25℃)

(Typical value measured at V_{DD}=5V, T_A=25°C, unless otherwise specified)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage		V_{DD}	-	4.5	5	5.5	V
Start voltage		V_{STUP}	-	-	-	2.8	V
UVLO		V_{UVLO}	-	2.3	-	-	V
Sustaining Voltage at OUT Ports		V_{OUT}	OUT_R/G/B[3:0]	-	-	V_{DD}+0.3	V
Supply Current		I_{DD1}	All channel on CG=111111	-	17.2	-	mA
		I_{DD2}	All channel on, CG=000000	-	12.1	-	
		I_{DD3}	SDB=low	-	0.1	-	µA
Switch On Resistance		R_{SWITCH}	I_{SWITCH}=1.5 A	-	168	333	mΩ
Output Current(R/G/B)		I_{OUT}	R_{EXT}=7.92KΩ, or use build-in resister	5	-	40	mA
Bit Skew(Channel)		dI_{OUT1}	I_{OUT}=5mA V_{OUT}=1.0V	-	±1.5	±3.0	%
		dI_{OUT2}	I_{OUT}=40mA V_{OUT}=1.0V	-	±1.5	±3.0	%
Chip Skew(IC)		dI_{OUT3}	I_{OUT}=5mA V_{OUT}=1.0V	-	±2.5	±5.0	%
		dI_{OUT4}	I_{OUT}=40mA V_{OUT}=1.0V		±2.5	±5.0	%
Output Current vs. Output Voltage Regulation		$\%/dV_{OUT}$	All channel on I_{OUT}=5~40mA V_{OUT}=1.0V~3.0V	-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	All channel on I_{OUT}=5~40mA V_{DD}=4.5~5.5V V_{OUT}=1.0V	-	±1.0	±2.0	%/V
Input Voltage	“H” level	V_{IH}	-	2.3	-	3.3	V
	“L” level	V_{IL}	-	GND	-	1	V
Output Voltage (MISO)	“H” level	V_{OH}	I_{OH}=-3mA	2.3	-	3.3	V
	“L” level	V_{OL}	I_{OL}=+3mA	GND	-	0.4	V
External Reference Voltage		V_{REXT}	-	-	1.2	-	V
Over Current Protection		V_{OCP}	-	-	V_{DD}-0.4	-	V
Over Temp Threshold		T_{OTP}	-	-	140	-	°C
Pull-down resistor		$R_{IN(DOWN)}$		-	100	-	KΩ

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Switching Characteristics (V_{DD}= 5.0V , Ta=25 ºC)

Output channel switching characteristics

(Typical value measured at V_{DD}=5V, T_A=25°C, unless otherwise specified)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal PWM clock frequency	f_{GCLK}	R_{EXT}=7.68KΩ V_{DS}=1V R_L=200Ω C_{VDD}=22uF (20mA) C_L=10pF C_1=0.1uF C_2=0.1μF C_{MISO}=10pF V_{LED}=5.0V	24.25	25	25.75	MHz
Rise time of output ports(fast)	$t_{OR(FAST)}$		-	20		ns
Fall time of output ports(fast)	$t_{OF(SLOW)}$		-	20		ns
Rise time of output ports(slow)	$t_{OR(FAST)}$			75		ns
Fall time of output ports(slow)	$t_{OF(SLOW)}$			75		ns

Output channel timing

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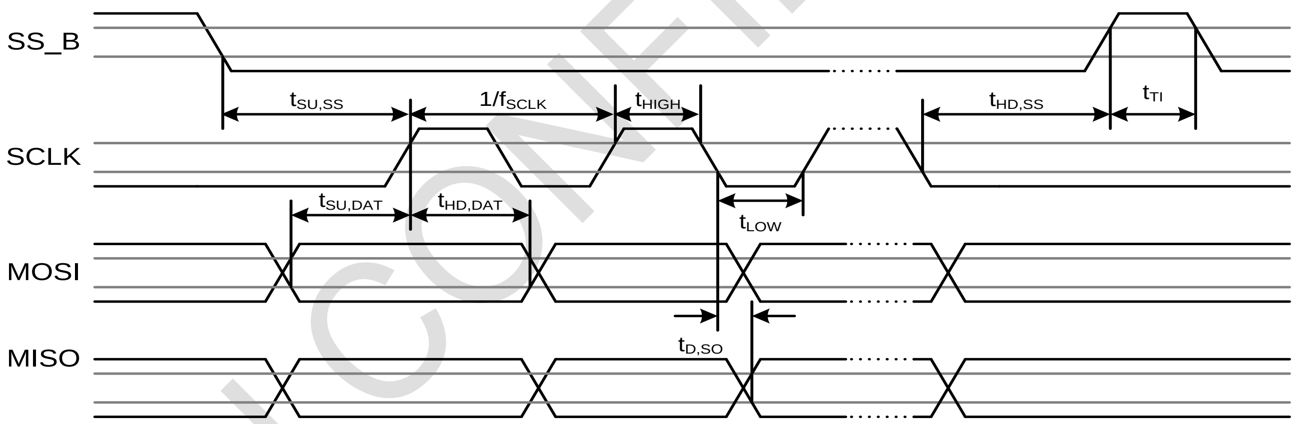
Interface switching characteristics

SPI

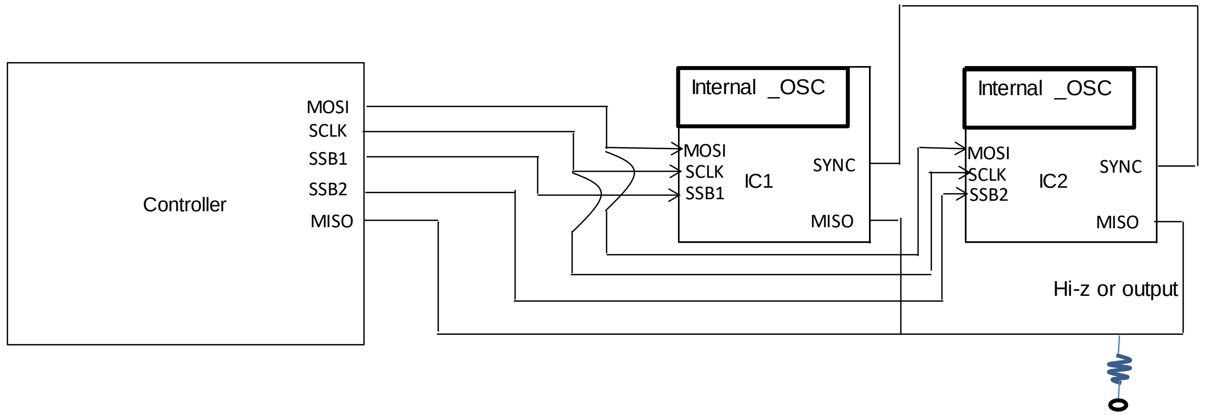
(Typical value measured at V_{DD}=5V, T_A=25°C, unless otherwise specified)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Data clock frequency	f_{SCLK}	R_{EXT}=7.68KΩ V_{DS}=1V R_L=200Ω C_{VDD}=22uF C_L=10pF C_1=0.1uF C_2=0.1μF C_{MISO}=10pF V_{LED}=5.0V	-	-	15	MHz
SCLK clock low period	t_{LOW}		33.33	-	-	ns
SCLK clock high period	t_{HIGH}		33.33	-	-	ns
Data setup time	$t_{SU,DAT}$		5	-	-	ns
Data hold time	$t_{HD,DAT}$		5	-	-	ns
Transceiving interval	t_{TI}		66.67	-	-	ns
Slave select setup time	$t_{SU,SS}$		4.25	5	5.75	ns
Slave select hold time	$t_{HD,SS}$		4.25	5	5.75	ns
MISO output time(Read mode only)	$t_{D,SO}$		-	-	15	ns

SPI serial bus timing

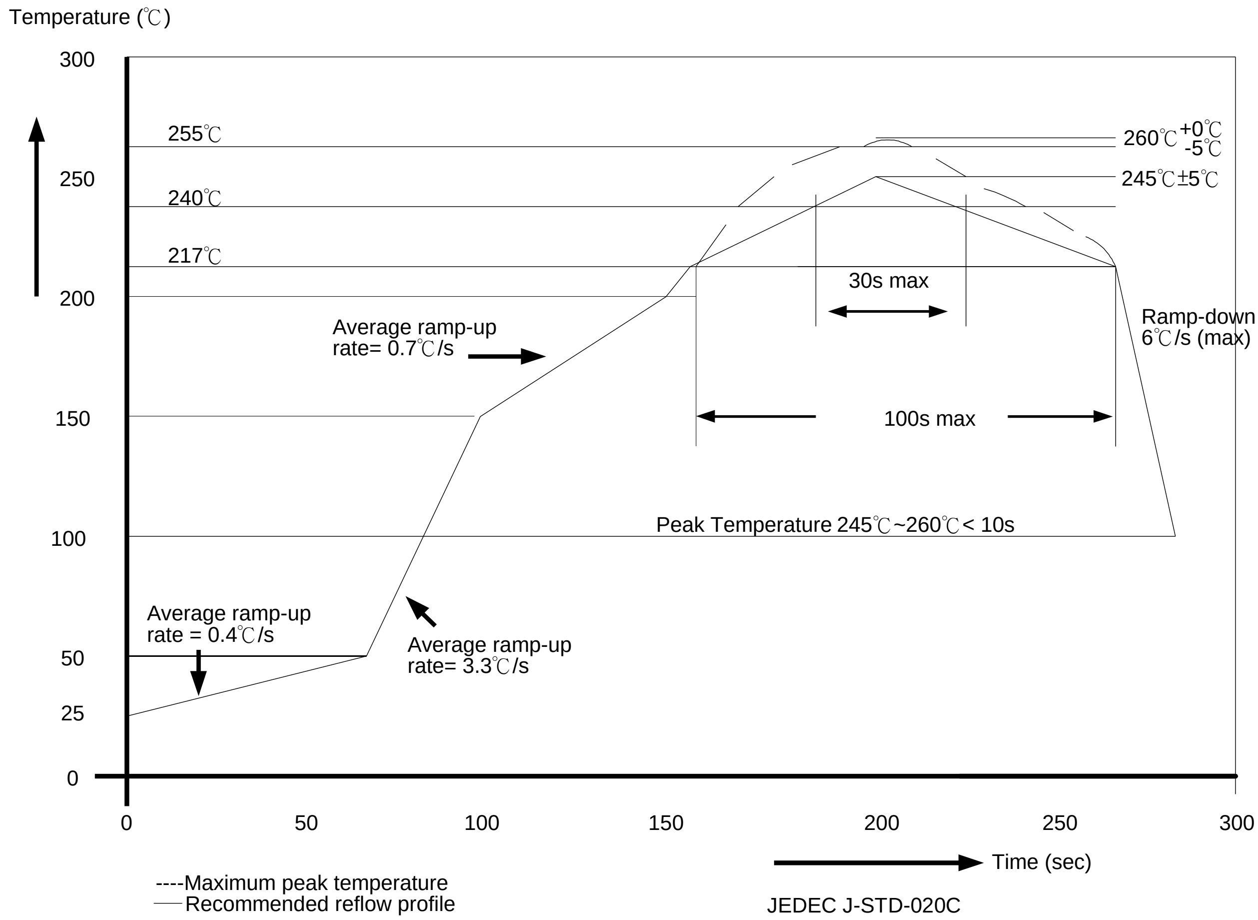


Application of SPI interface



Soldering Process of "Pb-free & Green" Package Plating*

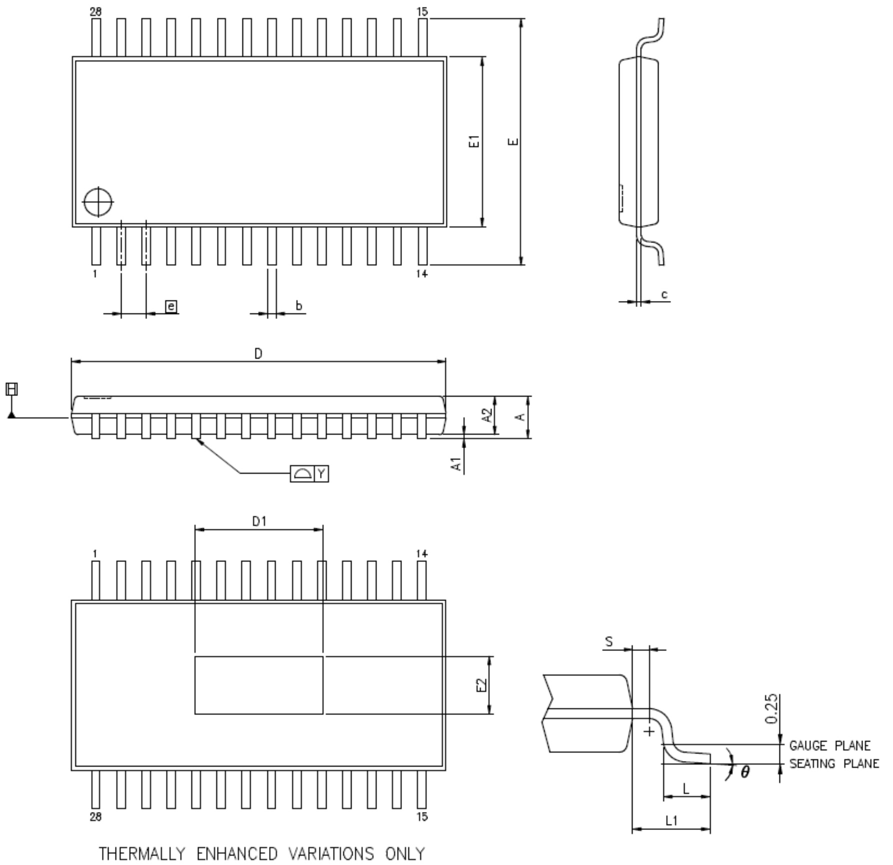
Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with the higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
105X14*	2.13	2.82	2.84	3.71

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代, 實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES:
1. JEDEC OUTLINE :
STANDARD : MO-153 AE REV.F
THERMALLY ENHANCED : MO-153 AET REV.F
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .

MBIA128GTS Outline Drawing

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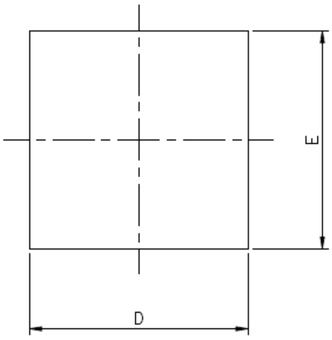

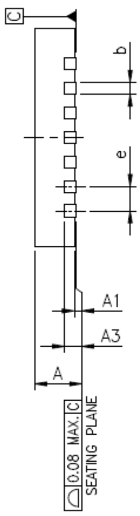

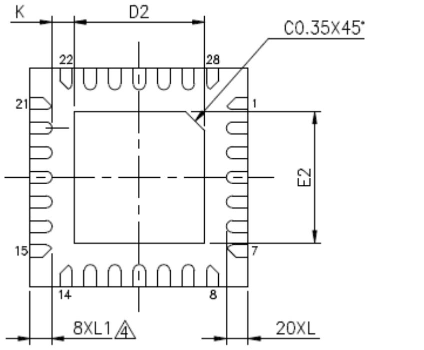

	PACKAGE TYPE					
JEDEC OUTLINE	N/A			N/A		
PKG CODE	WQFN(X428)			VQFN(Y428)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.17	0.22	0.27	0.17	0.22	0.27
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.45 BSC			0.45 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
△4 L1	0.33	0.38	0.43	0.33	0.38	0.43
K	0.20	—	—	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X114 MIL	2.30	2.40	2.45	2.30	2.40	2.45	V	X	N/A

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

MBIA128GFN Outline Drawing

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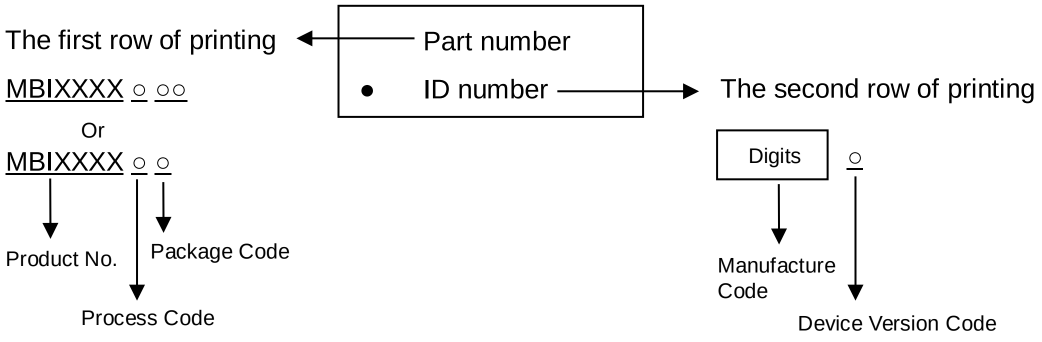
Product Top-mark Information



Product Revision History

Advance Information Version	Device Version Code
V0.01	T
V0.02	T
V0.03	T

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